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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,927	01/20/2004	Vincenzo DiTommaso	1482-173	2171

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,927	DITOMMASO, VINCENZO	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-10,12-15,17-20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-10,12-15,17-20,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 3-5, 7-10, 12-15, 17-20, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Xu (6,714,081).

Claim 1, Xu shows a bias circuit (2, Fig. 1) comprising: a reference cell (16, Fig. 1) to generate a bias signal (1M5)', and a first component (6) coupled to the reference cell to adjust the bias signal by replicating (col. 5, lines 15-16) a thermal characteristic of a second component (4) that may be coupled to the bias circuit, wherein the reference cell includes a feedback loop (12, 6, and 8) to drive a pair of transistors (26) and wherein the first component is arranged in the feedback loop (6 is coupled to 12 and 8 which arranged in feedback loop).

Claim 3, Xu shows a bias circuit according to claim 1 wherein the feedback loop comprises a current mirror (18 & 20, col. 5, lines 47-48) coupled between the first component (6) and the reference cell (16).

Claim 4, Xu shows a bias circuit according to claim 3 wherein the current mirror is arranged to load the reference cell (load to current IM3).

Claim 5, Xu shows a bias circuit according to claim 1 wherein the first component comprises a transistor (6 is a NMOS transistor).

Claim 7, Xu shows bias circuit according to claim 1 wherein the reference cell and the first component are coupled together at a summing node (a node among IM4, IM5, and IREF).

Claims 9-10, 12-13. The apparatus described above is applicable to the method claims 9-10, 12-13.

Claim 15, Xu shows a system comprising'. a first circuit comprising a reference cell (16, Fig. 1) to generate a bias signal, and a first component (6) coupled to the reference cell; and a second circuit coupled to the first circuit to receive the bias signal, the second circuit comprising a second component (4), wherein the first component is arranged to adjust the bias signal by replicating a thermal characteristic of the second component (col. 5, lines 15-16), wherein the reference cell includes a feedback loop (6, 12, and 8) to drive a pair of transistors (26), and wherein the first component is arranged in the feedback loop (6 is part of feedback loop).

Claim 17, Xu shows a system according to claim 15 wherein the feedback loop comprises a current mirror (20 & 18) coupled between the first component (6) and the reference cell (16).

Claim 18, Xu shows a system according to claim 15 wherein the reference cell and the first component are coupled together at a summing node (a node among IM4, IM5, and IREF).

Claim 19, Xu shows a system according to claim 15 wherein the first and second components have a matching thermal characteristic (the thermal characteristic is matched since 6 is replica of 4).

Claim 20, Xu shows a bias circuit comprising'. bias means for generating a bias signals wherein the bias means comprises a feedback loop (6, 8, and 12) arranged to drive a pair of transistors (26), and replication means (6) for replicating a thermal characteristic of a component (4) that may be coupled to the bias circuit, wherein the replication means comprises a replication component that is matched to the component that may be coupled to the bias circuit, wherein the replication component is arranged in the feedback loop (6 coupled to current IM2 and sense by 8 which is feedback to control current IM3).

Claim 23, Xu shows a bias circuit according to claim 20 further comprising means (a node among IM4, IM5, and IREF) for combining a signal from the bias means with a signal from the replication means.

Claim 24, Xu shows a bias circuit according to claim 20 further comprising means (12) for controlling the amount of compensation provided by the replication means.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 9, 14, 15, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Haefner et al (5,699,014).

Claim 1, Haefner shows a bias circuit (Fig. 7) comprising:

a reference cell (720 & 725) to generate a bias signal (V730 which is output bias signal V400); and

a first component (601 and 605) coupled to the reference cell to adjust the bias signal by replicating (col. 9, lines 41-45) a thermal characteristic of a second component (300 and 500) that may be coupled to the bias circuit,

wherein the reference cell includes a feedback loop (601, 605, 730, 710 are positive feedback) to drive a pair of transistors (720 and 725) and wherein the first component is arranged in the feedback loop (col. 9, lines 14-17 and col. 11, lines 56-63).

Claim 8, Haefner shows a bias circuit according to claim 1 further comprising a clamping circuit (760) coupled to the reference cell.

The limitations of claims 9, 14, 15, and 20 are rejected as above claims 1 and 8.

Claims 1, 8, 9, 14, 15, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Monticelli (4,618,816).

Claim 1, Monticelli shows a bias circuit (Fig. 7) comprising:

a reference cell (12, 13, 20, 15-16, 18) to generate a bias signal (at node 17); and

a first component (21) coupled to the reference cell to adjust the bias signal by replicating a thermal characteristic (value or W/L of transistors 21 and 24 are the same, see a table in column 5) of a second component (24) that may be coupled to the bias circuit,

wherein the reference cell includes a feedback loop (21, 22, 18 are negative feedback loop, col. 3, lines 38-39) to drive a pair of ΔVbe transistors (12 and 13) and wherein the first component is arranged in the feedback loop (21 is in the feedback loop).

Claim 3, Monticelli shows a bias circuit according to claim 1 wherein the feedback loop comprises a current mirror (22) coupled between the first component (21) and the reference cell.

Claim 5, Monticelli shows the first component comprises a transistor (21 is a transistor).

The limitations of claims 9, 10, 12, 15, 17, 19, 20 are rejected as above claims 1, 3, 5.

Response to Arguments

In response to Applicant's argument that neither Xu or Haefner transistor pair are base on the ΔVbe principle, Applicant misinterprets the principle that claims are interpreted in the light of the specification. Although the pair of transistor with other elements are connected in specific way to produce the ΔVbe principle are found as

examples or embodiments in the specification, the were not claimed explicitly. Nor were the words that are used in the claims defined in the specification to require these limitations. A reading of the specification provides no evidence to indicate that these limitations must be imported into the claims to give meaning to disputed terms.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

5/26/06

ANH Q. TRAN
PRIMARY EXAMINER